

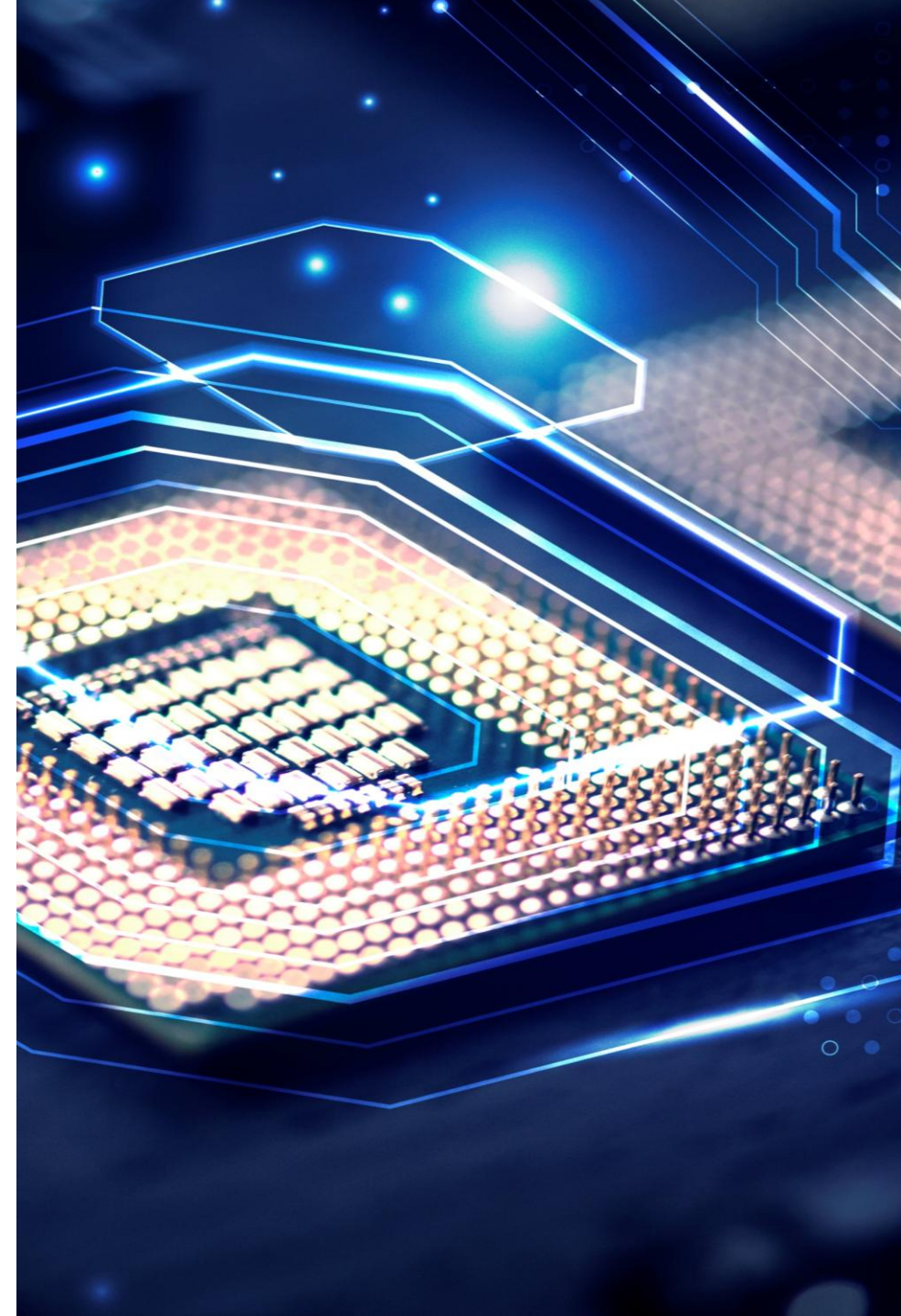
Verdancia Capital — **SPV₁**

Summary Overview

*Investing In the Strategic Advantage of a
Scarcity-Driven Supply Chain*

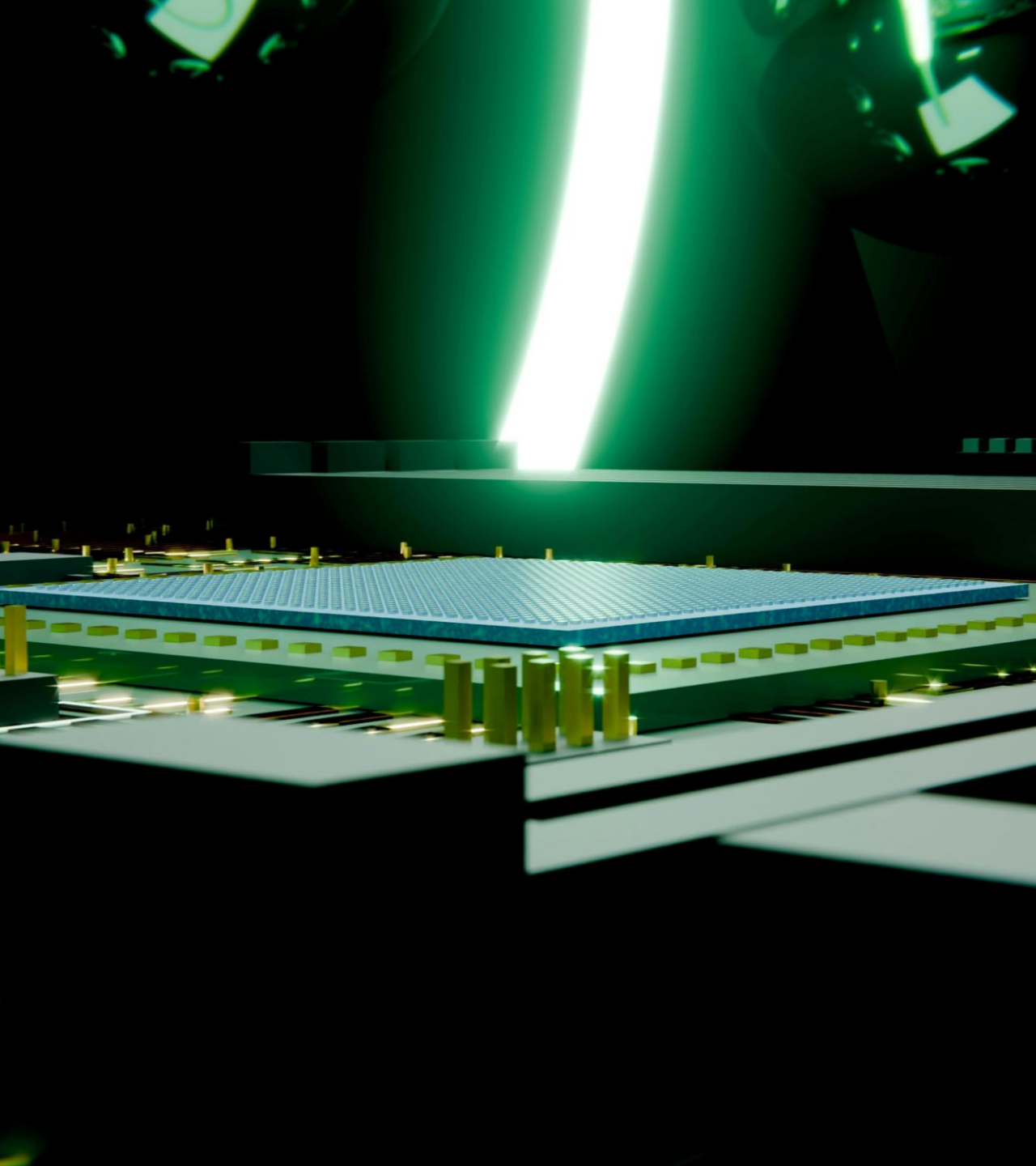
September 10, 2026

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Agenda

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- Introduction
 - Executive Summary
 - The Technology & Products
 - Advantages of Supply Chain Embeddedness
 - Funding Milestones & Timeline
 - Competitive Landscape in Brief
 - Closing



Introduction

- Verdancia's SPV1 ***targets a foundational transition*** in AI: demand for *inference compute* is entering a phase of structural and sustained long-term expansion.
- *Inference is what powers real-world AI applications; inference is where income is generated.*
- Verdancia's SPV1 is premised upon a fundamental scarcity: the ability to supply the needed inference infrastructure is structurally constrained by both technology and capacity.
- SPV1 aims to navigate supply chain constraints while outperforming its peers when introduced in 2027.

Executive Summary

- While training in AI has benefited from years of investment in high-power GPUs, ***purpose-built inference*** hardware is the next durable growth frontier.
- There has long been a technical issue associated with the hardware associated with inference: ***memory wall***. This is the bottleneck that even the best hardware still can't fully address.
- Verdancia's SPV investment targets a Taiwan-based founding team that has developed a new line of processors designed to perform inference efficiently by overcoming the memory wall. The team uses a novel technology, "***wafer-on-wafer***." This approach has demonstrated exceptional inference performance in terms of available memory, accessible bandwidth, and compute throughput.
- SPV1 has generated significant early interest among potential and long-term clients and partners. Projected adoption of SPV1's technologies and products is realistic, and adoption efforts are ongoing. More details are available upon request.

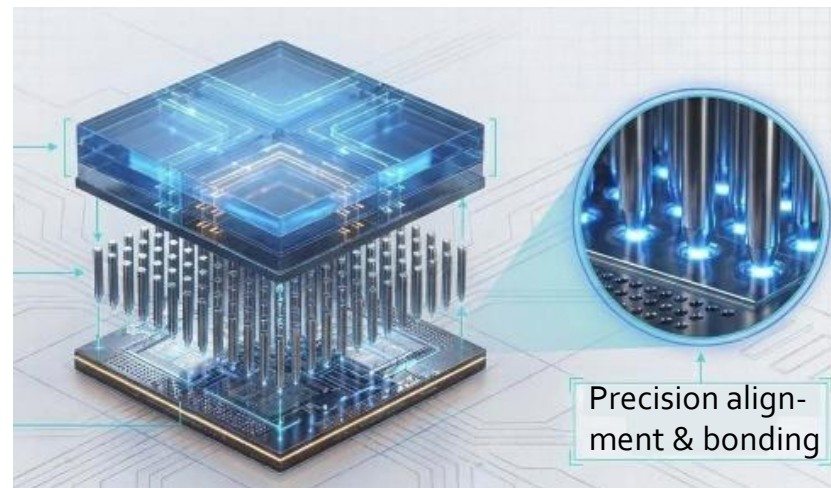
Executive Summary (Cont'd)

- Wafer-on-wafer is a craft that requires deep collaboration during conception, engineering, and fabrication. By being part of the supply chain fabric, the SPV company gains access to proven manufacturing capabilities.
- Furthermore, SPV₁ has secured the availability of ***scarce foundry and component support to ensure mass production.***
- Investment Highlights:
 - USD 50 million (20% of the target company; Post-money valuation: 250 million);
 - Projected investment period: six years, in a 4 + 2 configuration;
 - Expected return profile: MOIC: 4-5x, IRR: 30-40%.
- Investors will invest in a ***single-asset fund*** managed by Verdancia Capital. As such, they are subject to an annual management fee and profit-sharing with Verdancia upon exit.

The Technology & Products,

- When general-purpose GPUs perform inference, they run into the “memory wall”: data cannot move through the system fast enough to keep the GPU fully utilized. As a result, the GPU spends much time idle, burning power while waiting on data movement.
- Verdancia’s SPV target company (the “Company” or “Project”) employs a “wafer-on-wafer” architecture. The design stacks four layers of DRAM arrays, interconnected through specialty “pillars” that also *provide high-bandwidth vertical links* rather than relying on standard interconnects. These *memory layers are then bonded directly onto a custom SoC die, forming a unified compute-and-memory structure*. The configuration is shown below.

- 1) 4-DRAM Array -Stacked memory Layers L1-L4) →
- 2) GPIO Pillar →
- 3) Advanced SoC Die Featuring micro-Vias →



The Technology & Products

- When general-purpose GPUs are tasked with LLM inference, they must move enormous volumes of data through memory token-by-token. NVIDIA's current generation of GPU, for example, offers compute throughput of around 989 to 2,250 TFLOPS, yet inference does not require training-level compute, and the standard memory bandwidth of 4.8 to 8.0 TB/s is insufficient to feed the compute units at desirable levels.
- INFPRO₁, SPV₁'s first chip within the family, provides **up to 500 TFLOPS of compute throughput, 64 GB of memory, and 48 TB/s of memory bandwidth**, which compare favorably to what the competitors can currently offer.
- To facilitate large-scale adoption of the INFPRO family, the Company has developed fully integrated rack-level inference hardware built around the INFPRO chips, complete with proprietary software interface and compiler tools. Together, the software and the hardware can be readily applied within any existing data-center or model-serving environment. Datacenters and enterprises can deploy INFPRO-based racks without modifying their existing infrastructure.

Advantages of Supply Chain Embeddedness

- Wafer-on-wafer is a craft that requires deep collaboration along the conception, engineering, and fabrication processes, something that outside competitors cannot readily access. This approach ensures that engineering feasibility, performance targets, and cost structures are validated early and continuously. The SPV1 family of chips are a result of this collaboration amongst *the Target Company, Taiwan's main memory maker, and a key foundry.*
- In the case of INFPRO chips, Memory Maker must pre-fabricate the DRAM wafers to precise specifications so they can align and interconnect through nearly one million specialty GPIO pillars, *which also serve as high-bandwidth vertical links.* Once the memory module is completed, Key Foundry will need to fabricate the SoC and bond it to the stacked memory wafers, a process that likewise requires exact alignment and specification compliance. In other words, ***"wafer-on-wafer" is custom fabrication taken to a deeper level.***
- Then there is the issue of foundry and component scarcity. Due to longstanding relationships, *both Memory Maker and Key Foundry have committed to providing DRAM wafers and foundry capacity, respectively, in support of full production* once the Project reaches the production stage. These commitments represent critical assurances for the Company and materially strengthen the Project's viability.



Funding Milestones & Timeline

- The Investment shall be funded in three tranches, the first shall be provided upon Closing, with the latter two subject to the achievement of development and pre-production execution milestones. Please note that the timeline for **the capital calls assume a November 15th, 2026, Closing**. Milestone details are provided post-NDA.
- The development phases of the project are complete, production execution is the next focus. The milestones are designed and arranged to facilitate the start of mass-production (MP) in 4Q 2027.

Capital Call timeline:

- I. Tranche I: Initial funding of USD 15 million **will be provided upon Closing**.
- II. Tranche II: Capital call for the second tranche, in the amount of USD 20 million, is scheduled between **February 1st and March 31st, 2027**.
- III. Tranche III: For USD 15 million, capital call is scheduled between **June 1st and July 31st, 2027**.

Competitive Landscape In Brief

Company (country)	Chip Name/Architecture	Peak Compute Throughput	Memory Bandwidth	On-chip Memory Capacity
INFPRO (Taiwan)	INFPRO1 / 2 / 4 (3D- DRAM ASIC)	1,000 – 4,000 TFLOPS	48.0 – 192.0 TB/s	64 – 256 GB 3D- DRAM
Etched(U.S.)	Soho(Trans-former)	~2,000 TFLOPS	~5.0 TB/s	144 GB HBM3e
FuriosaAI (Kor)	RNGD (SRAM + LPDDR5X)	512 TOPS	~1.5 TB/s	512MB SRAM + 48GB LPDDR
Rebellions (Kor)	Rebel (LLM NPU / HBM3)	~1,000 TFLOPS	~2.0 – 3.2 TB/s	32 – 64 GB HBM3
Tenstorrent (U.S.)	Wormhole (RISC-V + Tensix)	~1,000 TOPS (INT8)	~1.6 TB/s (GDDR6)	32 – 64 GB GDDR6
d-Matrix (U.S.)	Jayhawk (In-compute memory DIMC)	~1,000 TFLOPS (MXFP6)	High on-chip bandwidth	~100s MB SRAM + external
DeepX (Kor)	DX-M1 / V3 (低功耗 NPU)	~200 – 500 TOPS	~512 GB/s	16 – 32 GB LPDDR5
Hailo (Israel)	Hailo-10 / 15 (數據流 NPU)	~40 – 100 TOPS	Low on-chip bandwidth	8 – 16 GB LPDDR4/5

- The table here provides performance metrics for the competitors within the inference chip space. As stated, SPV1 family compare favorably to the peers. Please refer to the WORD document for a second table regarding project status and valuation information. The list of names is not exhaustive and leaves out some ongoing projects that are not close to market entry or for proprietary use.



Closing

- As a single-asset vehicle, SPV1 offers LPs a clear test case for observing Verdancia's disciplined evaluation and execution process.
- With a differentiated position in the supply chain, SPV1 benefits from structural advantages that strengthen both feasibility and upside.
- The opportunity is compelling: demand for inference capacity is set to grow far faster than global supply, creating room for credible providers to capture meaningful share, ***especially considering the valuation where SPV1 is conducting this financing.***

Thank You!

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